WHAT IS CLAIMED IS:

1. An input/output buffer operative in an analog mode and a digital mode, comprising:

a pad;

a digital signal line which includes a transmission gate connected to the pad;

an analog signal line connected to the pad;

an analog/digital mode controller which sets an output level of the digital signal line in the analog mode;

a transmission gate controller which controls the transmission gate when a signal voltage of the pad exceeds a reference voltage.

2. The input/output buffer of claim 1, wherein the digital signal line further includes a first resistor connected between the pad and the transmission gate, an output driver having an output connect to the transmission gate, a Schmitt trigger having an input connected to the transmission gate, and an input driver having an input connected to an output of the Schmitt trigger.

3. The input/output buffer of claim 2, wherein the analog signal line includes a second resister connected to the pad.

4. The input/output buffer of claim 3, further comprising a constant voltage tolerance unit connected to the pad, wherein the constant voltage tolerance unit includes first and second PMOS transistors connected in series between a power supply voltage and the ground voltage, the first PMOS transistor having a gate connected to the pad and the second PMOS transistor having a gate connected to the power supply voltage.

5. The input/output buffer of claim 4, wherein the power supply voltage is a second power supply voltage, and wherein the transmission gate controller includes:

a third PMOS transistor having a source connected to the pad and a gate connected to a first power supply voltage, and receiving a well bias voltage from a connection node of the first and second PMOS transistors of the constant voltage tolerance unit;

a first NMOS transistor having a drain connected to a drain of the third PMOS transistor and a gate connected to the second power supply voltage; and

a second NMOS transistor having a drain connected to a source of the first NMOS transistor, a source connected to the ground voltage, and a gate connected to the output of the Schmitt trigger.

6. The input/output buffer of claim 5, wherein the transmission gate includes:

a third NMOS transistor connected between the second resistor and the Schmitt trigger and gated to the second power supply voltage; and

a fourth PMOS transistor connected between the second resistor and the Schmitt trigger and gated to the drain of the third PMOS transistor, and receiving the well bias voltage from the connection node of the first and second PMOS transistors of the constant voltage tolerance unit.

7. The input/output buffer of claim 2, wherein the output driver comprises a PMOS transistor and an NMOS transistor, which are connected in series between a power supply voltage and the ground voltage, the PMOS transistor and the NMOS transistor having gates connected to an internal output signal and a complementary internal output signal, and drains connected between the transmission gate and the Schmitt trigger.

8. The input/output buffer of claim 2, wherein the analog/digital mode controller comprises:

an inverter which receives an analog/digital control mode signal; and

a PMOS transistor connected between a power supply voltage and the output of the Schmitt trigger and gated to an output of the inverter.

9. An input/output buffer operative in an analog mode and a digital mode, comprising:

a pad;

a digital signal line which includes a first transmission gate connected to the pad;

an analog signal line which includes a second transmission gate connected to the pad;

an analog/digital mode controller which sets an output level of the digital signal line in the analog mode;

a transmission gate controller which controls the first and second transmission gates when a signal voltage of the pad exceeds a reference voltage.

10. The input/output buffer of claim 9, wherein the digital signal line further includes a first resistor connected between the pad and the first transmission gate, an output driver having an output connect to the first transmission gate, a Schmitt trigger having an input connected to the first transmission gate, and an input driver having an input connected to an output of the Schmitt trigger.

11. The input/output buffer of claim 10, wherein the analog signal line further includes a second resister connected between the pad and the second transmission gate.

12. The input/output buffer of claim 11, further comprising a constant voltage tolerance unit connected to the pad, wherein the constant voltage tolerance unit includes first and second PMOS transistors connected in series between a power supply voltage and the ground voltage, the first PMOS transistor having a gate connected to the pad and the second PMOS transistor having a gate connected to the power supply voltage.

13. The input/output buffer of claim 12, wherein the power supply voltage is a second power supply voltage, and wherein the analog/digital controller comprises:

a first inverter which receives an analog/digital control mode signal;

a third PMOS transistor connected between the second power supply voltage and an output of the Schmitt trigger and gated to an output of the first inverter;

a second inverter which receives an output of the first inverter;

a level shifter which shifts an amplitude swing of the output of the first inverter;

a fourth PMOS transistor having a source connected to a first power supply voltage and a gate connected to an output of the second inverter; and

a fifth PMOS transistor having a source connected to the second power supply voltage, a drain connected to a drain of the fourth PMOS transistor, and a gate connected to an output of the level shifter.

14. The input/output buffer of claim 13, wherein the transmission gate controller comprises:

a sixth PMOS transistor connected to a well bias voltage and having a source connected to the pad and a gate connected to the drain of the fourth PMOS transistor of the analog/digital controller;

a first NMOS transistor having a drain connected to a drain of the sixth PMOS transistor and a gate connected to the second power supply voltage; and

a second NMOS transistor having a drain connected to a source of the first NMOS transistor, a source connected to the ground voltage, and a gate connected to the output of the second inverter of the analog/digital controller.

15. The input/output buffer of claim 14, wherein the first transmission gate comprises:

a third NMOS transistor connected between the first resistor and the Schmitt trigger and gated to the second power supply voltage; and

a seventh PMOS transistor connected to the well bias voltage and connected between the first resistor and the Schmitt trigger and gated to the drain of the sixth PMOS transistor of the transmission gate controller.

16. The input/output buffer of claim 14, wherein the second transmission gate includes:

a third NMOS transistor connected between the second resistor and an internal analog signal node and gated to the second power supply voltage; and

a seventh PMOS transistor connected to the well bias voltage and connected between the second resistor and the internal analog signal node and gated to the drain of the first PMOS transistor of the transmission gate controller.

17. The input/output buffer of claim 10, wherein the output driver comprises a PMOS transistor and an NMOS transistor, which are connected in series between a power supply voltage and the ground voltage, the PMOS transistor and the NMOS transistor having

gates connected to an internal output signal and a complementary internal output signal, and drains connected between the transmission gate and the Schmitt trigger.